REMARKS

Claims 41 and 48 are amended. New claims 62-70 are added. Claims 41-70 are pending in the application.

The Examiner requests a new title indicative of the invention to which the claims are directed. The title was amended in the Preliminary Amendment filed February 5, 2002 to recite "Integrated Circuit Device". Such recitation is essentially verbatim the preamble of the independent claims as originally filed, and therefore, the title is clearly indicative of the invention to which the claims are directed. Applicant respectfully requests withdrawal of this request in the next office action.

Claims 41-50, 53-56 and 58-61 stand rejected under 35 U.S.C. §102(e) as being anticipated by Corisis et al. (U.S. Patent No. 6,284,571).

Claims 51, 52 and 57 are objected to as being dependent upon a rejected base claim.

New claims 69-70 include the limitations of objected to claims 51 and 52, respectively, and the limitations of the rejected base claim from which claims 51-52 originally depended, and therefore, claims 69-70 are allowable. Applicant respectfully requests allowance of claims 69-70 in the next office action.

Regarding the anticipation rejection against claim 41, such claim recites a housing encapsulating at least a portion of a heat sink and positioned between substantially an entirety of the heat sink and semiconductor die. Corisis teaches a semiconductor die 200; a lead frame 202 secured on the semiconductor die

200 by dielectric tape 223; and a voltage reference plane 250 secured on the lead frame 202 by dielectric material 248 (col. 7, lines 15-40; Fig. 2). In no fair or reasonable interpretation does Corisis teach or suggest a housing encapsulating at least a portion of a heat sink and positioned between substantially an entirety of the heat sink and semiconductor die as recited in claim 41. Accordingly, Corisis fails to teach or suggest a positively recited limitation of claim 41, and therefore, claim 41 is allowable. Applicant respectfully requests allowance of claim 41 in the next office action.

Claims 42-47 depend from independent claim 41, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are not taught or shown by the art of record.

Regarding the anticipation rejection against claim 48, such claim recites a heat sink positioned in heat-receiving relation with a semiconductor die and comprising leads extending outward of a housing and configured to release heat outside the housing. Figs. 1-2 of Corisis teach lead fingers 104/204 of lead frame 102/202 extend from a transfer molded plastic package 108/208 "to pass signals between the integrated circuitry of die 100/200 and external circuitry (not shown)" (col. 5, lns. 55-63 and col. 7, lns. 15-19; Figs 1-2). That is, Corisis explicitly teaches the lead fingers 104/204 and lead frame 102/202 are "to pass signals." Corisis also teaches a voltage reference plane 250 may act as a heat sink (col. 7, lns. 35-37). However, the voltage reference plane 250 is insulated

from lead frame 202 by dielectric material 248 (col. 7, lns. 26-28). Additional teachings of Corisis are directed to increasing the heat sink transfer properties of the voltage reference plane 250 by reconfiguring the same, for example, see Fig. 3 and column 7, lines 42-58 wherein voltage reference plane 250 is provided with projections 270 that do not extend outward of the housing (Fig. 3). Accordingly, considering the four corners of the document, Corisis **only** teaches or suggests lead fingers extend from a transfer molded plastic package "to pass signals between the integrated circuitry of a die and external circuitry." Consequently, in no reasonable or fair interpretation does Corisis teach or suggest a heat sink comprising leads extending outward of the housing as recited in claim 48. In particular, the statement on pg. 4 of paper no. 3 that lead 204 conducts heat externally of the housing 208 is in error and contrary to the specific teachings of Corisis which indicates the teachings to projections 270 are for heat transfer from die 200 (col. 7, lns. 42-59; Fig. 3). Leads 204 **conduct signals and not** heat as alleged by the Examiner. Further, Corisis teaches dielectric 248 insulates the signaling leads 204 from the voltage reference plane 250. Accordingly, Corisis fails to teach or suggest a positively recited limitation of claim 48, and therefore, claim 48 is allowable. Applicant respectfully requests allowance of claim 48 in the next office action.

Claims 49-52 depend from independent claim 48, and therefore, are allowable for the reasons discussed above with respect to the independent claim,

as well as for their own recited features which are not taught or shown by the art of record.

Regarding the anticipation rejection against claim 53 (please note that such is incorrectly referred to as claim 48 at pg. 4 of paper no. 3), such claim recites a first lead frame and a second lead frame comprising a heat sink. The Examiner states Fig. 2 of Corisis teaches a first lead frame 204 extending from a right side of the package (pg. 4 of paper no. 3) and refers to **the same** lead frame 204 to state such teaches a second lead frame extending from a left side of the package (pg. 5 of paper no. 3). Respectfully, the Examiner is mistaken as reference numeral 204 refers to lead fingers and reference numeral 202 refers to a single lead frame (col. 7, lns. 15-19; Figs. 1-2). It is clear references 202 or 204 do not disclose or suggest a second lead frame comprising a heat sink as claimed. Corisis teaches lead fingers 204 and lead frame 202 of Fig. 2 is the same as previously described LOC configuration, obviously referring to Fig. 1 (col. 7, lns. 16-19). Fig. 1 of Corisis shows a **single unit frame** 102. Accordingly, in no fair or reasonable interpretation does Corisis teach a first lead frame **and** a second lead frame as recited in claim 53. Further, Corisis fails to disclose or suggest any lead frame structures which comprise a heat sink. For these reasons, Corisis fails to teach or suggest a positively recited limitation of claim 53, and therefore, the claim is allowable. Applicant respectfully requests allowance of claim 53 in the next office action.

Claims 54-62 depend from independent claim 53, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are not taught or shown by the art of record.

This application is now believed to be in immediate condition for allowance, and action to that end is respectfully requested. If the Examiner's next anticipated action is to be anything other than a Notice of Allowance, the undersigned respectfully requests a telephone interview prior to issuance of any such subsequent action.

Respectfully submitted,

Dated: 11-14-02

By: _____
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Application Serial No. 10/072,417
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Group Art Unit 2826
Examiner ..... Pershelle Greene
Attorney's Docket No. MI22-1939
Title: Integrated Circuit Device (As Amended)

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO AUGUST 14, 2002 OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

41. (Amended) An integrated circuit device comprising:

a semiconductor die comprising synchronous-link dynamic random access memory circuitry;

a heat sink thermally coupled with ~~to~~ the semiconductor die; and

a housing encapsulating at least a portion of the heat sink and positioned between substantially an entirety of the heat sink and semiconductor die.

48. (Amended) An integrated circuit device comprising:

a housing enclosing a semiconductor die comprising memory circuitry; and

a heat sink positioned in heat-receiving relation with the semiconductor die and comprising leads extending outward of the housing and configured to release heat outside the housing.

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